2.4 A 33.6-to-33.8Gb/s Burst-Mode CDR in 90nm CMOS

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To realize the optical point-to-multipoint communication systems, the multi-Gb/s burst-mode CDR circuit plays one of the important roles [1, 2]. For PON applications, each asynchronous packet has to be correctly received within several tens of bit times. Conventional PLL-based CDR circuits suffer from the long settling time. In this paper, a 33.6-to-33.8Gb/s full-rate burst-mode CDR circuit in 90nm CMOS technology is presented.

The proposed burst-mode CDR circuit is shown in Fig. 2.4.1. It is composed of an input matching circuit, differential microstrip lines, a phase selector, a retimed D flip flop (DFF), a wideband data buffer, 2 clock buffers, 2 *LC* gated VCOs (GVCOs), and a PLL. To transmit multi-tens Gb/s data into a chip, a wideband input matching circuit is indispensable. The proposed input matching circuit is shown in Fig. 2.4.2. The input symmetric transformer is used to absorb the pad capacitance. The shunt peaking circuit is realized by 2 symmetric transformers and resistors to enhance the bandwidth. The 50Ω differential microstrip lines made of metal 9 on top of metal 1 is used to absorb the routing capacitance. The simulated -3dB bandwidth of this input matching circuit is up to 70GHz.

Conventional GVCOs [1, 2] are widely used in burst-mode CDR circuits. In [1], the ring oscillator are gated and stopped by input data. It needs a long startup time to re-oscillate for a multi-tens GHz GVCO. In [2], a short and accurate delay is needed to trigger the GVCO for the recovered clock generation, and it is difficult to realize in the multi-tens GHz circuits. To improve the above issues, the proposed *LC* GVCO is shown in Fig. 2.4.3. It is composed of 2 *LC* delay stages and a data-triggering multiplexer. When the input data, D_{in}, is high, the upper *LC* delay stage and the multiplexer realize a 2-stage *LC* ring oscillator and the clocks come from 2 *LC* delay stages are in phase. Once the input data changes to low, the lower *LC* delay stage and the multiplexer form another oscillator and the output of the upper *LC* stage tracks with that of the lower *LC* stage. Thus, no oscillator is stopped during the normal operation. It will significantly reduce the data-dependent jitter. The simulated gain of this GVCO is around 1GHz/V, while consuming 9.6mA. To reduce the frequency error, a replica GVCO (i.e., GVCO2) and a PLL is realized as shown in Fig. 2.4.1. Note that the oscillation frequency of both GVCOs is adjusted by MOS varactors. This PLL is composed of a differential PFD, differential-to -single-ended (D-to-S) voltage-to-current converter (V/I) [3], and a divide-by-8 divider.

Since the full-rate GVCO is adopted in this burst-mode CDR circuit, this GVCO may lock with the rising or falling edge of the input date. To recover the correct data, a phase selector is utilized as shown in Fig. 2.4.1. It is composed of a multiplexer, a current-mode logic DFF and a delay, τ_d, which is realized by an LC delay stage. Assume that the falling edge of the GVCO1 locks with the input data and the rising edge of the GVCO1 is selected to retime the data. However, if the rising edge of the GVCO1 locks with the input data, the complementary output of the GVCO1 is used to retime the data. While this phase selector generates a constant logic high or low, it allows the multiplexer to select the correct clock and retime the data. Note that the requirement of τ_d is not stringent. It allows the input data to sample the delayed clock far away from the clock transitions.

The design of the output data buffer is important. Once its bandwidth is not wide or the gain is not flat, it may induce significant jitters. The conventional BJT-based Cherry-Hooper amplifier is widely utilized for these purposes. To realize a 40Gb/s data buffer, Fig. 2.4.4 shows the proposed output data buffer. The Cherry-Hooper amplifier is combined with the inductive peaking technique. Its small-signal model is equivalent to a 4th-order *LC* Butterworth network [4]. In Fig. 2.4.4, the asymmetric 2:1 transformer is used to realize L_1 and L_2, and the symmetric 1:1 transformers are used to realize L_3 and L_4. The simulated -3dB bandwidth of this data buffer is 55.7GHz. The simulated jitter of this data buffer is 0.0032UI for a 40Gb/s, 2^{31}-1 PRBS. This buffer draws 11mA from a 1.2V supply.

This proposed burst-mode CDR circuit is fabricated in 90nm CMOS technology. Figure 2.4.5 shows a die micrograph; the chip occupies 0.8×0.8mm^2 including the on-chip loop filter and pads. It consumes 73mW and 98mW with and without buffers, respectively, from a 1.2V supply. This CDR circuit recovers data between 33.6 and 33.8Gb/s. Figure 2.4.6(a) shows the measured single-ended recovered data for a 33.72Gb/s, 2^{11}-1 PRBS. The measured peak-to-peak and rms jitters for the recovered data are 7.56ps and 1.15ps, respectively. The measured operational range for the output clock of the PLL is 33.5 to 34.5GHz. The measured output spectrum of the PLL output clock at 33.72GHz is shown in Fig. 2.4.6(b). The measured phase noise at 1MHz offset frequency is -87.2dBc/Hz. To demonstrate the burst-mode transient behavior, the user-defined bit sequence is used. The measured recovered data and clock are shown in Fig. 2.4.7. This CDR circuit can tolerate 31 consecutive identical bits with a locking time of 0.2ns (< 7b).

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[3] J. Savoj and B. Razavi, "A 10 Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection," *ISSCC Dig. Tech. Papers*, pp. 78-79, Feb., 2001.
[4] C. Lee and S. I. Liu, "A 35Gb/s Limiting Amplifier in 0.13μm CMOS Technology," *Symposium on VLSI Circuits Dig.,* pp. 152-153, June, 2006.

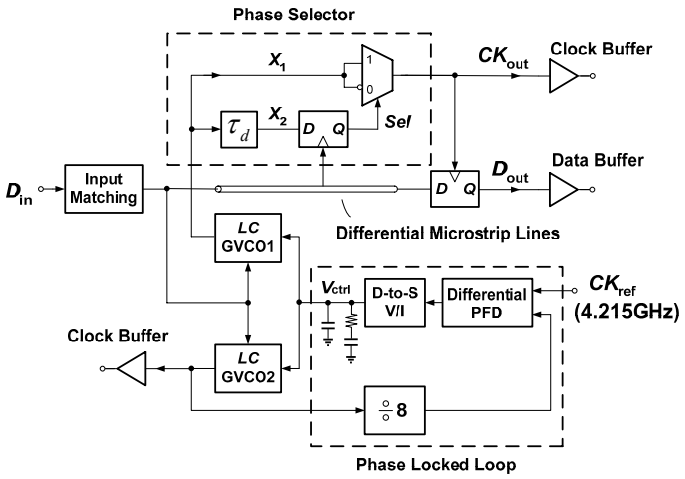


Figure 2.4.1: Burst-mode CDR circuit.

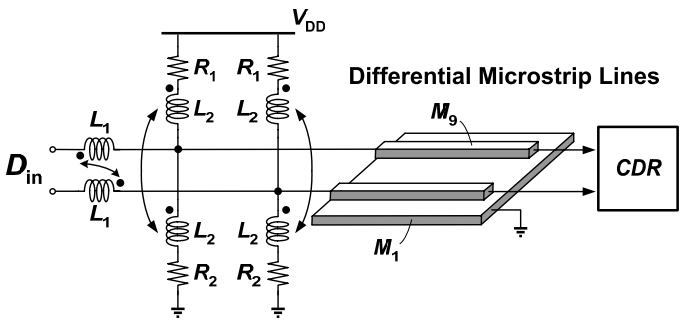


Figure 2.4.2: Input matching circuit.

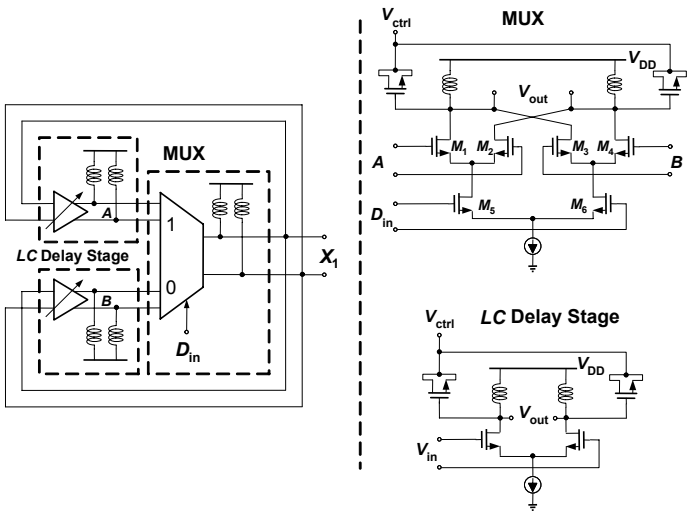


Figure 2.4.3: LC GVCO.

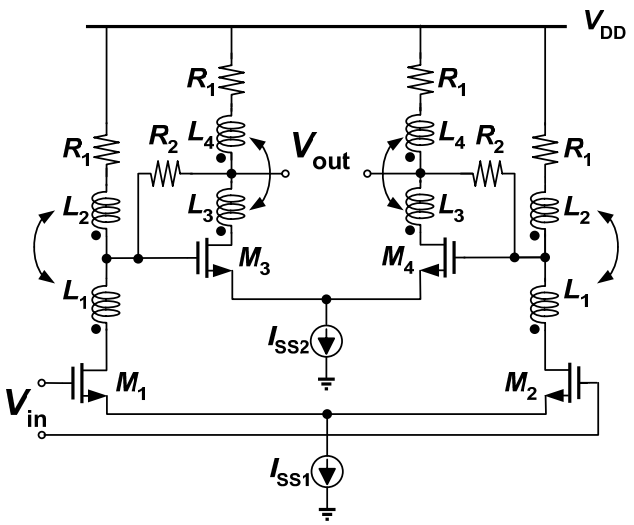


Figure 2.4.4: Wideband data buffer.

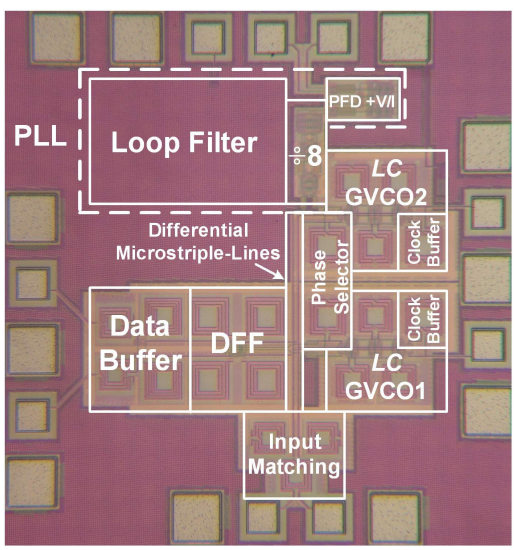
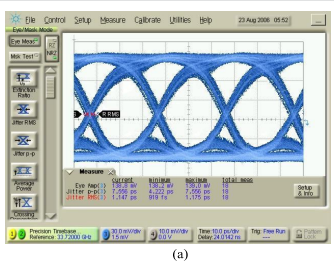
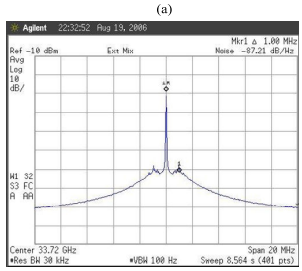


Figure 2.4.5: Die micrograph.



(a)



(b)

Figure 2.4.6: (a) Measured recovered data.
(b) Measured spectrum for the PLL output clock.

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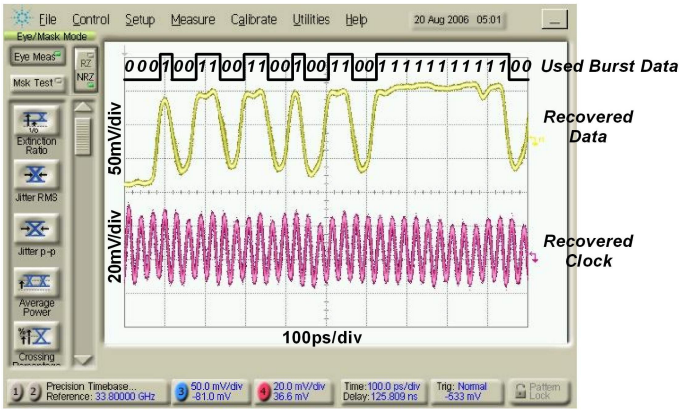

Figure 2.4.7: Measured burst-mode transient response.

